CONTROL DATA
MP-32
COMPUTER SYSTEMS

DEVELOPMENT HISTORY

MP-32 COMPUTER SYSTEM DEVELOPMENT HISTORY 01/16/79.

THE PURPOSE OF THIS DOCUMENT IS TO GIVE A GENERAL HISTORY OF THE MP-32 HARDWARE AND SOFTWARE DEVELOPMENT, FOR THOSE ANALYSTS WHO WILL WORK ON MP-32 SOFTWARE PROGRAMS.

IN 1970, AEROSPACE DIVISION (ASD) DEVELOPED A HARDWARE ARCHITECTURE KNOWN AS THE MICRO-PROGRAMMABLE PROCESSOR (MPP). THE MPP DESIGN IS VERY MODULAR IN NATURE. IT COMES IN TWO VERSIONS: A 16-BIT VERSION AND A 32-BIT VERSION. THE 16-BIT VERSION WAS USED TO DEVELOP A CDC 1700 EMULATOR FOR THE MILITARY MARKET. BY DOING THIS, THE AEROSPACE DIVISION WAS ABLE TO DELIVER A COMPUTER SYSTEM WITH A LARGE SOFTWARE BASE WITHOUT THE ASSOCIATED COSTS IN DEVELOPING THAT SOFTWARE, BECAUSE THEY WERE ABLE TO USE ALL OF THE 1700 SYSTEM SOFTWARE AVAILABLE FROM THE COMMERICAL DIVISONS.

THE SUCCESS OF THE MPP PROMPTED THE CORPORATION TO EMBARK ON A PROJECT TO REPACKAGE THE MILITARIZED MPP INTO A COMMERICAL PACKAGE UTILIZING COMPONENTS THAT WERE LESS COSTLY THAN THE MILITARY VERSION. THE TWO UNITS WERE CALLED THE MP-16 AND MP-32 ENGINES.

THE PRIME IMPETUS BEHIND THE MP-16 ENGINE WAS TO BE A 1700 EMULATOR, AND THE GOAL FOR THE MP-32 ENGINE WAS TO REPLACE HARDWIRED CONTROLLERS IN APPLICATIONS NEEDING EXTREMELY HIGH BANDWIDTH.

THE CYBER 18 IS AN OUTGROWTH OF THAT MP-16 ENGINE EMULATING THE 1700 AND IS NOW THE STANDARD MINI-COMPUTER WITHIN THE CORPORATION.

THE MP-16 ENGINE (AGAIN EXECUTING A 1700 INSTRUCTION SET, BUT WITH SIGNIFICANT ADDITIONS TO THAT INSTRUCTION SET FOR COMMUNICATIONS) IS THE BASE HARDWARE FOR THE 2550 COMMUNICATIONS PROCESSOR AVAILABLE ON THE CYBER 170 LINE.

THE MP-32 ENGINE ORIGINALLY WAS DESIGNED TO BE A CONTROLLER, AND ONLY NEEDED A MEMORY INTERFACE TO PROVIDE BUFFERING FOR THE PERIPHERAL DEVICES IT WAS TO BE CONTROLLING. THIS MEMORY ADDRESSING CAPABILITY WAS ONLY 8192 WORDS LONG. THE EFFORT IN DEVELOPING THE MP-32 HARDWARE WAS PRIMARILY TO INCREASE THE MP-32 ENGINE'S MEMORY ADDRESSING CAPABILITY.

TO MORE FULLY UNDERSTAND THE MP-32 SOFTWARE DEVELOPMENT, ONE MUST FOLLOW ASD'S 32-BIT MPP HARDWARE AND SOFTWARE DEVELOPMENT. IN 1974, ASD USED THEIR 32-BIT MPP TO EMULATE A MACHINE CALLED THE MP-60. THIS EMULATOR WAS ORIGINALLY DEVELOPED FOR A PROGRAM FOR THE U.S. ARMY CALLED ARTADS. THIS SYSTEM WAS DEVELOPED AROUND THE PHILOSOPHY OF USING MULTIPLE

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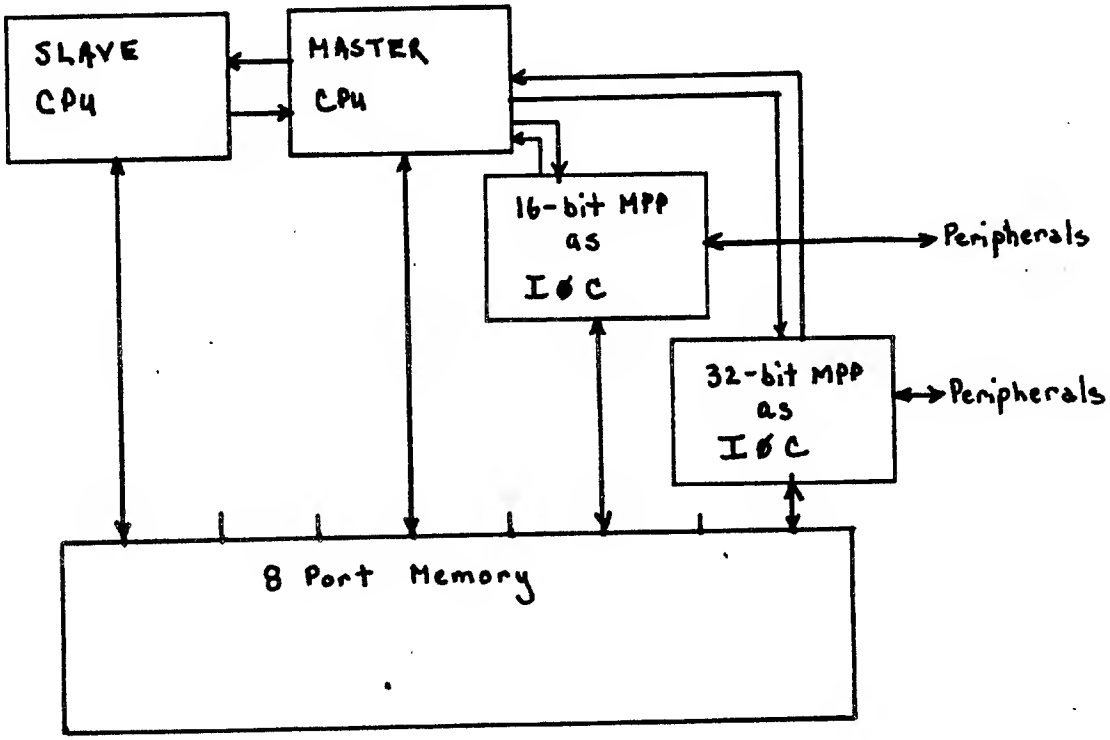
PROCESSORS SUPPORTED BY A STANDARD OPERATING SYSTEM. THIS EMULATION CAPABILITY AND THIS OPERATING SYSTEM, CALLED MP-60 AND MPX/RT, WERE THE BEGINNINGS OF THE MACRO PRODUCT SET USED ON THE MP-32.

THE ORGINAL MP-60 (MPP) CONFIGURATION WAS DIVIDED INTO THREE TYPES OF PROCESSOR ELEMENTS, MASTER CPU, SLAVE CPUS, AND INPUT/OUTPUT CONTROLLERS. A TYPICAL MP-60 (MPP) COMPUTER SYSTEM IS DIPICTED BELOW: (IØCs).



IN ARTADS THE MASTER CPU WAS AN MP-60 EMULATOR WHILE THE SLAVE CPUS WERE LITTON 3050 TACFIRE EMULATORS. THE INPUT/OUTPUT CONTROLLERS, WERE USED FOR THE FOLLOWING REASONS:

- ISOLATION OF I/O HARDWARE FROM THE COMPUTATIONAL UNITS.
- ISOLATION OF I/O SOFTWARE OVERHEAD FROM THE COMPUTATIONAL UNITS.
- DEVICE INDEPENDENT I/O DEFINITIONS.

THE MPX/RT OPERATING SYSTEM ALLOWES THE CONCURRENT EXECUTION OF TWO JOBS:

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1. BACKGROUND JOBS

   BACKGROUND JOBS EXECUTE IN PAGED PROGRAM STATE 1 AND COMMUNICATE WITH THE MPX/RT EXECUTIVE SERVICE FUNCTIONS VIA MONITOR CALLS. THE BACKGROUND TASKS CANNOT USE THE MONITOR STATE PRIVILEGED INSTRUCTIONS OR REFERENCE MEMORY OCCUPIED BY THE EXECUTIVE.

2. FOREGROUND JOBS

   FOREGROUND JOBS ARE INITIALIZED IN PAGED PROGRAM STATE 1 AND EXECUTE IN NON-PAGED PROGRAM STATE 4 AND/OR MONITOR STATE 0.

   FOREGRAOUND TASKS COMMUNICATE WITH THE MPX/RT EXECUTIVE VIA MONITOR CALLS. IN ADDITION, FOREGRACUND TASKS HAVE ACCESS TO CERTAIN MPX/RT TABLES AND ROUTINES.

AT THIS TIME THREE PROGRAMS WERE BEING ACTIVELY MARKETED WHERE A COMMERICAL VERSION OF THE MP-60 COMPUTER SYSTEM WAS PROPOSED. IT WAS BELIEVED THE MP-32 ENGINE COULD BE MODIFIED TO MEET THE REQUIREMENTS FOR A COMMERCIAL MP-60 COMPUTER SYSTEM. THE SUNNYVALE PSD GROUP BEGAN THE TASK OF BUILDING THE CONCEPTUAL PRE-PRODUCTION PROTOTYPE AND ESTABLISHING THE MARKET PLACE.

IN PARALELL WITH THE HARDWARE DEVELOPMENT, SOFTWARE TOOLS WERE DEVELOPED ON THE CYBER AS WELL AS THE MP-60 (MPX/RT) EMULATOR. THE NEXT STEP WAS TO QUICKLY DEVELOP AN INPUT/OUTPUT CONTROLLER (IOC) REPLACEMENT USING EXISTING HARDWARE FOR THE CYBER 18. AS IT TURNS OUT THE IOC CONCEPT DEVELOPED BY ASD IS EXPENSIVE BECAUSE EACH NEW CUSTOMER MUST PAY FOR BOTH THE IOC FIRMWARE AND HARDWARE DEVELOPMENT.

THE FOLLOWING GROUND RULES WERE USED IN THE QUICK DEVELOPMENT OF AN IOC REPLACEMENT:

1. USE EXISTING CYBER 18 PERIPHERALS.
2. WRITE I/O DRIVERS FOR THESE PERIPHERALS WHICH EXECUTED IN STATE 7.
3. MAKE MINIMAL MODS TO THE MPX/RT OPERATING SYSTEM.
4. MAKE THE IOC REPLCAEMENT AUTONOMOUS TO THE MPX/RT OPERATING SYSTEM.
5. CHANGE AND EXPAND THE MP-60 INSTRUCTION SET (TRAP EXISTING I/O COMMANDS).
6. DO IT AS FAST AS POSSIBLE, RE-WRITE IT LATTER AT THE CUSTOMER'S EXPENSE.

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THERE WERE MANY DRAWBACKS TO THE ABOVE APPROACH:

1. PSD PERSONNEL DID NOT HAVE A WORKING KNOWLEDGE OF MPX/RT WHICH DICTATED MAKING MINIMAL MODS TO MPX/RT OPERATING SYSTEM.
2. AUTONOMOUS HARDWARE IS DIFFICUIT TO SIMULATE WITH AUTONOMOUS SOFTWARE.
3. THE PHILOSOPHY OF DO IT FAST RESULTED IN MANY REHASHES OF THE MP-60 EMULATOR AND DRIVERS.

MAKING MINIMAL MODS TO MPX/RT OPERATING SYSTEM.
2. AUTONOMOUS HARDWARE IS DIFFICULT TO SIMULATE WITH AUTONOMOUS SOFTWARE.
3. THE PHILOSOPHY OF DO IT FAST RESULTED IN MANY REHASHES OF THE EMULATOR AND DRIVERS.

THERE WAS ALSO MANY HARDWARE PROBLEMS RESULTING FROM THE DMA INTERFACE, WHICH FINALLY REQUIRED THE DISK DRIVER TO READ BACK AND COMPARE ALL INFORMATION WRITTEN ONTO THE DISK.

DURING THE IOC REPLACEMENT DEVELOPMENT ONE OF THE THREE CUSTOMERS PICKED THE ASD MP-60 HARDWARE AND PSD WAS GIVEN A CONTRACT TO MODIFY THE MPX/RT OPERATING SYSTEM FOR THEIR CONFIGURATION AND APPLICATION. THIS GREATLY IMPROVED PSD'S UNDERSTANDING OF THE MPX/RT OPERATING SYSTEM AND ITS DEFICIENCES. DURING THIS PSD CONTRACT THE MP-32 WAS PROPOSED AS PART OF A LARGE CYBER CONFIGURATION AND CORPORATE FUNDING WAS ALLOCATED TO LA JOLLA TO BUILD TWO PRODUCTION PROTOTYPES.

THE SOFTWARE DEVELOPMENT GROUP AT ASD WAS DEVELOPING A NEW OPERATING SYSTEM MPX/MP. MPX/MP WAS A TRUE MULTI-PROGRAMMING OPERATING SYSTEM BUT WAS ONLY USED AS A STEPPING STONE TO MPX/MC (LATER CHANGED TO MPX/OS). THE MPX/OS IS A MULTI-TASKING, MULTI-PROCESSING, AND MULTI-PROCESSOR SYSTEM. THE MPX/OS VERSION WAS IMMEDIATELY CHOSEN TO BE THE NEW BASELINE OPERATING SYSTEM FOR THE MP-32 COMPUTER SYSTEM.

THE MPX/OS VERSION INVALIDATED MANY OF THE GROUND RULES USED IN THE MPX/RT IOC REPLACEMENT DEVELOPMENT. IN ADDITION, HARDWARE CHANGES WERE MADE WHICH ELIMINATED SOME OF THE AUTONOMOUS HARDWARE SIMULATION. THE FOLLOWING GROUND RULES WERE USED TO MODIFY (KLUDGE) THE I/O SUBSYSTEM INTO MPX/OS:

1. MINIMAL MODIFICATIONS TO EXISTING DRIVERS.
2. MAKE MPX/OS FORGET STATE 7.
3. CHANGE DRIVERS TO RUN IN STATE 0.
4. CHANGE AND EXPAND THE MP-60 INSTRUCTION SET.
5. DO IT AS FAST AS POSSIBLE, RE-WRITE LATER AT

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CUSTOMER'S EXPENSE.

THE ABOVE GROUND RULES INCREASED THE NUMBER OF DEFICIENCIES ALREADY IN THE I/O SUBSYSTEM. IN SUMMARY, THE PRESENT I/O SUBSYTEM IS NOT JUST A SINGLE KLUDGE BUT A KLUDGE OF A KLUDGE. IN ORDER FOR NEW FEATURES TO BE IMPLEMENTED, PSD HAS A WELL DESIGNED MP-32 I/O SUBSYTEM, HOPEFULLY ELIMINATING THE REQUIREMENT FOR FUTURE KLUDGES.

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News

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CONTROL DATA CORPORATION

For Release: Immediately

MICROPROGRAMMABLE COMPUTER ARRAY FRONT-ENDS CONTROL DATA CYBER 170 SYSTEMS

MINNEAPOLIS, MN, May 27, 1977 -- Control Data Corporation has announced a special medium-scale computer that can be tailored to the data acquisition and reduction applications of computer installations that include its large-scale CYBER 170 systems.

This new system, based on a 32-bit microprogrammable processor designated the Control Data MP-32, is targeted for highly specialized pre-processing applications such as telemetry data acquisition and manipulation, data editing and compression, and the processing of repetitive algorithms.

The results of this preprocessing activity then are passed to an interconnected CYBER 170 system for further, higher level data processing.

Control Data's MP-32 system consists of a set of computer hardware components that can include up to 16 million bytes of main memory in separate one-megabyte chassis. Each memory can be accessed by from one to eight separate MP-32 processors, the company said, to permit as many as 128 combinations of processors sharing main memory in a single system.

(more)

The basic MP-32 processor contains 4,096 instructions of user-programmable, read-write micromemory and 288 general purpose registers. Interconnection of the central processor and main memory is accomplished by means of an asynchronous memory controller.

The memory controller contains 1,024 address relocation registers, memory protection and management logic, and a memory request register set that can contain up to four concurrent memory requests.

Options available for the basic processor include expansion of micromemory up to 8,192 instructions and increasing the number of processing registers from the basic 288 to a total of 8,480 in 2,048-register increments.

Main storage -- the one or more multi-port memory units -- features 600-nanosecond dynamic MOS memory that can be increased in blocks of 128,000 bytes to a maximum of 16 million bytes. Asynchronous memory bank logic and the high-bandwidth design of the two to eight memory ports per chassis provide an effective data transfer rate of up to 26.6 million bytes per second for each memory unit.

MP-32 Software

Software available with the MP-32 includes packages hosted on the interconnected CYBER 170 system as well as programs, an operating system and utilities provided with the host MP-32.

(more)

Included is an operating system, designated MPX, that runs in single- or multiple-processor environments. The MPX system provides concurrent multiprogramming and multitasking of user jobs.

In addition to MPX, the MP-32 software product set includes a Fortran compiler, Compass macro-assembler, utility programs and interactive de-bugging aids. Under MPX, job execution can be allocated across 256 priority levels; in a typical user job mix a high priority real-time job could be combined with additional tasks being multiprogrammed with various Fortran compile and execute jobs.

In a multiprocessor configuration, the MPX operating system also can direct concurrent master and slave processor operations. Different processors can be assigned various tasks within a single job, resulting in parallel task execution.

CYBER 170 software supporting the MP-32 consists of an interactive assembler and simulator that can be used to develop MP-32 microprograms. Connection of the front-end system to CYBER 170 computers is supported by software in both systems. This permits job spooling into and out of the MP-32 through the CYBER 170, and enables the CYBER system to support MP-32 software development by means of its extensive source editing and interactive features, Control Data said.

(more)

Pricing, Availability

The MP-32 systems will be available in the fourth quarter of 1977 on a purchase-only basis, and a minimum configuration sells for $199,851. This system includes a single processor with a 4,098-instruction micromemory; 256,000 bytes of main memory; disk, printer, tape and card reader peripherals; and operator console and a CYBER 170 channel coupler.

An expanded system with eight MP-32 processors, 2 million bytes of main memory and the same complement of peripherals sells for $988,751.

The company also will provide systems engineering, integration and installation support under separate contract. This will ensure that the appropriate hardware, software and controlware elements are configured to a customer's specific application needs.

CDC mid-size system for data acquisition

Designated the Control Data MP-32, this medium-scale computer can be tailored to the data acquisition and reduction applications of computer installations that include CDC's Cyber 170 systems. Based on a 32-bit micro-programmable processor, the MP-32 is targeted for specialized pre-processing applications such as telemetry data acquisition and manipulation, data editing and compression, and the processing of repetitive algorithms. The MP-32 system consists of a set of computer hardware components that can include up to 16 million bytes of main memory in separate one-megabyte chassis. Each memory can be accessed by from one to eight separate MP-32 processors, to permit as many as 128 combinations of processors sharing main memory in a single system. The MP-32 systems will be available in the fourth quarter of 1977 on a purchase-only basis, and a minimum configuration sells for $199,851.

Control Data Corp., Box O, Minneapolis, MN 55440. (612) 853-4656.

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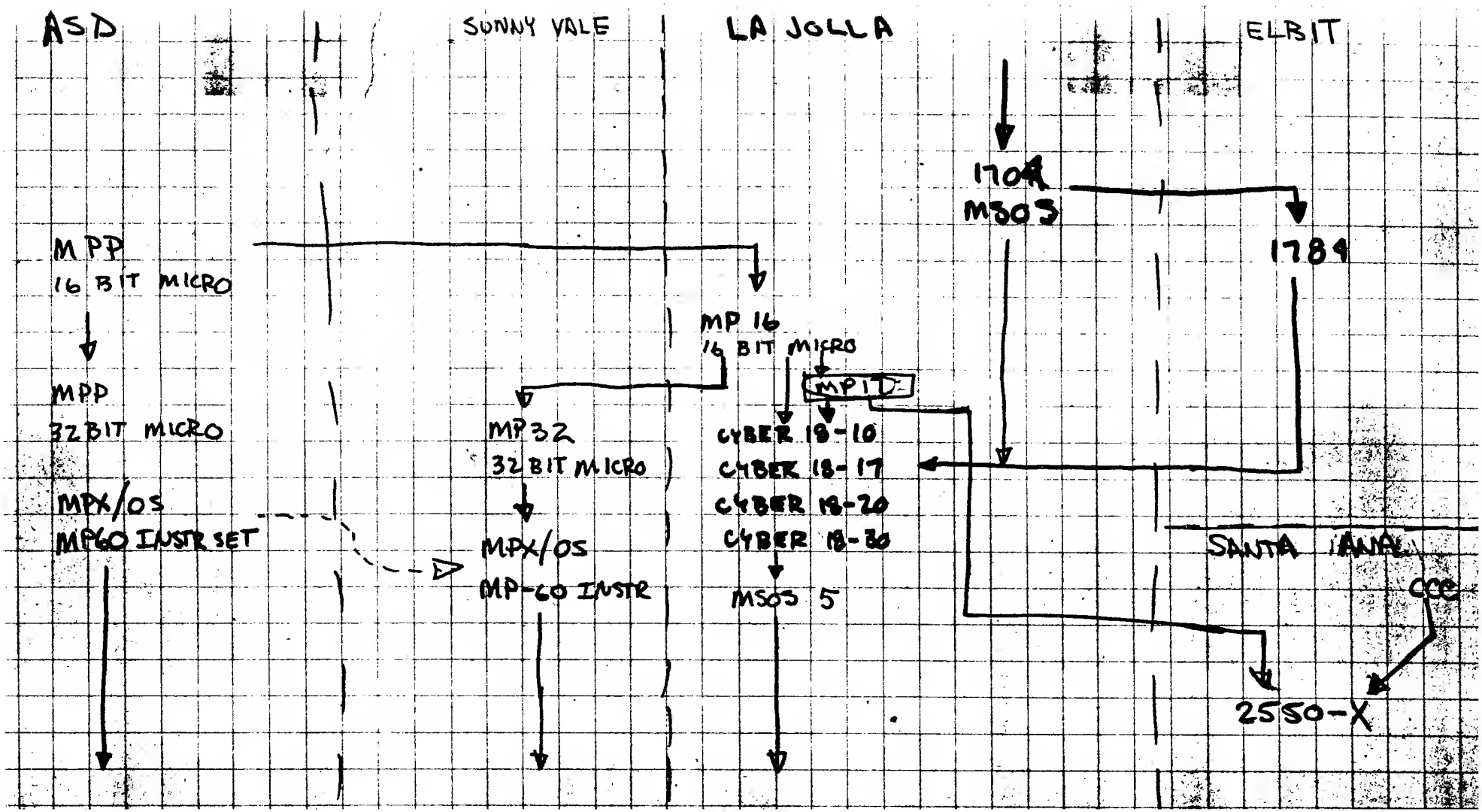
ASD
SUNNY VALE
LA JOLLA
ELBIT
1704
MS05
1784
MPP
16 BIT MICRO
MPP
32BIT MICRO
MPX/OS
MP60 INSTR SET
MP 16
16 BIT MICRO
MPIT
MP32
32 BIT MICRO
MPX/OS
MP-60 INSTR
CYBER 18-10
CYBER 18-17
CYBER 18-20
CYBER 18-30
MS05 5
SANTA ANA
CCC
2550-X